[c2]

[c3]

[c4]





CLAIMS

I/We claim:

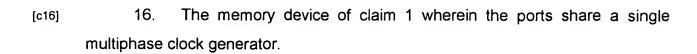
[c1] 1. A memory device comprising:

a memory; and

- a plurality of ports for accessing the memory of the memory device, each port having a serial communications link for receiving from and transmitting to an accessing device, each port using plesiosynchronous technique to receive symbols and using in-band symbols to transmit data and out-of-band symbols to transmit control information.
- 2. The memory device of claim 1 wherein each serial communications link is connected to an accessing device via a point-to-point connection.
- 3. The memory device of claim 1 wherein the plesiosynchronous technique oversamples data received via the serial communications link.
- 4. The memory device of claim 1 wherein each port includes a line driver with a fixed driver portion and a variable driver portion for DC-balancing.
- [c5] 5. The memory device of claim 1 wherein the memory includes multiple banks and wherein multiple banks can be simultaneously accessed by different ports.
- [c6] 6. The memory device of claim 5 wherein each bank includes multiple sections and wherein the multiple sections can be simultaneously accessed by different ports.

- [c7] 7. The memory device of claim 1 wherein the memory includes a bank with multiple sections and wherein the multiple sections can be simultaneously accessed by different ports.
- [c8] 8. The memory device of claim 7 wherein the multiple sections of the bank are configurable on a port-by-port basis.
- [69] 9. The memory device of claim 8 wherein the configuration information indicates to enable certain sections of the bank.
- [c10] 10. The memory device of 1 wherein the ports are connected to the memory using time-division multiplexing.
- [c11] 11. The memory device of claim 1 wherein the ports are connected to the memory using a crossbar switch.
- [c12] 12. The memory device of claim 1 wherein control information is transmitted as a primitive.
- [c13] 13. The memory device of claim 12 wherein a primitive includes two outof-band symbols.
- [c14] 14. The memory device of claim 12 wherein control information includes a synchronization symbol.
- [c15] 15. The memory device of claim 1 wherein the plesiosynchronous technique includes inserting or removing symbols to compensate for variations between clock frequencies of the accessing device and the memory device.

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- [c17] 17. The memory device of claim 16 wherein the multiphase clock generator is a phase lock loop.
- [c18] 18. The memory device of claim 1 wherein an out-of-band symbol is a synchronization symbol that encodes a memory command.
- [c19] \ \19. A memory device comprising:

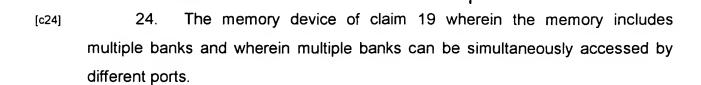
a memory that reads and writes data;

a multiphase clock generator that provides a multiphase clock signal; and a plurality of ports, each port for connecting to a serial communications link and for receiving data and control information via the serial communications link using a plesiosynchronous technique, wherein each port uses the generated multiphase clock signal generated by the multiphase clock generator.

[c20] 20. The memory device of claim 19 wherein data is sent using in-band symbols and control information is sent via out-of-band symbols.

- [c21] 21. The memory device of claim 19 wherein each serial communications link is connected to an accessing device via a point-to-point connection.
- [c22] 22. The memory device of claim 19 wherein the plesiosynchronous technique oversamples data received via the serial communications link.
- [c23] 23. The memory device of claim 19 wherein each port includes a line driver with a fixed driver portion and a variable driver portion for DC-balancing.

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- [c25] 25. The memory device of claim 24 wherein each bank includes multiple sections and wherein multiple sections can be simultaneously accessed by different ports.
- [c26] 26. The memory device of claim 19 including multiple sections and wherein multiple sections can be simultaneously accessed by different ports.
- [c27] 27. The memory device of claim 26 wherein the multiple sections are configurable on a port-by-port basis.
- [c28] 28. The memory device of claim 27 including the configuration information storage.
- [c29] 29. The memory device of 19 wherein the ports are connected to the memory using time-division multiplexing.
- [c30] 30. The memory device of claim 19 wherein the ports are connected to the memory using a crossbar switch.
- [c31] 31. The memory device of claim 19 wherein control information is transmitted as a primitive.
- [c32] 32. The memory device of claim 31 wherein a primitive includes two outof-band symbols.

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- [c33] 33. The memory device of claim 31 wherein control information includes a synchronization symbol.
- [c34] 34. The memory device of claim 19 wherein the plesiosynchronous technique includes inserting or removing symbols to compensate for variations between clock frequencies of the accessing device and the memory device.
- [c35] 35. The memory device of claim 19 wherein the multiphase clock generator is a phase lock loop.
- [c36] 36. The memory device of claim 19 wherein a synchronization symbol encodes a memory command.